

14 Carbon Nanotube Electronics and Optoelectronics

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Carbon nanotube field-effect transistors (CNFETs) are already competitive in some respects with state-of-the-art silicon transistors, and are promising candidates for future nanoelectronic devices. However, it is difficult to form ohmic contacts to carbon nanotubes, and most of the CNFETs reported to date operate as Schottky barrier transistors rather than conventional FETs. The electrostatics at the contact of a metal to a nanotube leads to device behavior very different from conventional transistors. In this chapter we discuss the consequences of Schottky barriers in CNFETs with respect to the scaling of transistor performance with reduced device size and the application of CNFETs as optoelectronic devices.

14.1 Introduction

Aggressive down-scaling of conventional silicon transistors over the past decades has led to characteristic device sizes below 100 nm in today's computer chips. Because of the associated problems, such as the increase of power consumption and device leakage current densities, there is intense interest in finding new materials and alternative devices. Carbon nanotubes are very promising in this respect, because of their exceptional structural, electronic, and optical properties ([1], see also Chap. 13). In particular, they exhibit ballistic transport over length scales of several hundred nanometers. Nanotube devices can be integrated with existing silicon-based structures. And recently, optoelectronic nanotube devices of nanometer dimensions and with tunable optical characteristics have emerged. In this chapter, we focus on the use of single-wall semiconducting carbon nanotubes in electronic devices such as field-effect transistors or in optoelectronic applications such as light-emitting devices.

Since the first demonstration of carbon nanotube field-effect transistors (CNFETs) in 1998 [2, 3] intensive research has led to a great improvement of device fabrication techniques and their transport properties. Today, CNFETs are already becoming competitive with state-of-the-art silicon transistors in

several aspects. For example, CNFETs using a top gate led to comparable turn-on voltages and superior transconductance [4], CNFETs with high- k dielectrics showed subthreshold slopes close to the thermal limit [5], and ballistic transport in CNFETs has been demonstrated [6, 7]. Even the first logic gate – a basic building block of a computer chip – has been created from a single carbon nanotube [8].

Despite their similarity to conventional devices, there is now ample evidence that CNFETs generally operate by an entirely different principle [9–13]. This is due to the presence of a Schottky barrier at the metal-nanotube contact, and the very different electrostatics of the quasi-one-dimensional nanotube compared to a planar interface. Important consequences include non-ideal switching behavior [11], unexpected scaling relations of device performance as its size is reduced [14] and new applications such as light emission from a single undoped nanotube (NT) [15].

14.2 Schottky Barrier Carbon Nanotube Transistors

At most metal-semiconductor contacts there is a Schottky barrier (SB), i.e. an energy barrier for carrier transport, which can be a severe limitation for devices. In semiconductor devices, this problem is generally avoided by replacing metal contacts with heavily doped regions of the semiconductor. However, nanotube devices have generally relied on direct metal-semiconductor contacts. Nonetheless, good device performance can be obtained. The reason is that the Schottky barrier represents a much less severe limitation for CNFETs than for conventional FETs, due to the quasi-one-dimensional (1D) geometry [11].

Another important difference is that in planar metal-semiconductor junctions, the Schottky barrier height is usually a substantial fraction of the bandgap, regardless of the metal used or other details. This is because the Fermi level at the interface is “pinned” deep in the bandgap by “metal-induced gap states” (MIGS)¹ in the semiconductor near the interface [16]. However, because of the very different electrostatics of the quasi-1D geometry, the MIGS are far less effective in pinning the Fermi level at nanotube-metal contacts [17]. The barrier height at NT contacts is therefore strongly affected by the local work functions of the metal and the nanotube. Thus the device properties can be dramatically modified by altering the work function near the contact, e.g. by exposure to oxygen or other gases.

Initially, only p-type transport was observed in CNFETs [2, 3] and led to the assumption that there is a vanishing barrier to the valence band of the

¹MIGS possess a complex wave vector and their wave function decays exponentially in the semiconductor with distance from the interface. They lie in the semiconductor bandgap and are forbidden in the bulk because their wave function rises infinitely in one direction. However, at an interface they can be attached to Bloch states of the metal in this direction and become valid solutions.

NT. Transistor action would then occur due to the modulation of the channel conductance as depicted in Fig. 14.1(a). At large positive gate voltages, the holes travelling from the drain to the source contact face a high potential barrier in the channel and the current is suppressed. The transistor is in its off-state. As the gate voltage is lowered, charge accumulates in the channel and the barrier is reduced. A significant current starts to flow and the transistor turns on. If the channel is ballistic the current modulation with gate voltage is governed only by the number of electrons with sufficient thermal energy to overcome the potential barrier. The current thus rises exponentially with gate voltage in the regime between the off- and the on-state (turn-on regime). The ratio between on- and off-current can be several orders of magnitude.

However, the finding of ambipolar conduction in CNFETs [9, 10], the transition from p- to n-type conduction upon gas adsorption [8, 18], and local gating of the CNFET at the contact [19] led to the notion that SBs must play a significant role. Transistor action due to the modulation of a SB has already been proposed for silicon based FETs [20] and has been demonstrated experimentally. In a SB-FET, the conduction of the device results from the modulation of the contact resistance as shown in Fig. 14.1(b). A SB of height ϕ_B at the nanotube-metal contact represents a potential barrier to charge carriers trying to enter from the source.² At zero gate voltage, only charge carriers thermally excited above the SB can enter the NT, the current is marginal, and the NT transistor is off. Upon a positive gate voltage, the SB to the conduction band is thinned down and thermally assisted tunneling of electrons from the source sets in. This tunneling current becomes significant only if the electric field due to the applied gate voltage can shrink the SB width down to a few nanometers. Analogously, holes can tunnel into the valence band at negative gate voltages. The transistor thus turns on at both negative and positive gate voltages and is in the off-state at intermediate voltages.

The SB assumption qualitatively explains ambipolar conduction, however, the observed output characteristics (I vs. V_d) of CNFETs show a linear slope at low drain voltages typical for a conventional transistor. For a SB transistor in the planar silicon geometry such a linear regime – desirable for many device applications – is unattainable. Thus an adequate model of the SB-CNFET must explicitly take the special properties of the NT such as quasi-1D electrostatics and the NTs electronic structure into account.

Recently, devices with small or vanishing Schottky barrier heights have been reported using Pd or Al contacts [6, 21]. However, relatively large diameter NTs (2 to 3 nm) with correspondingly small bandgaps (0.4 to 0.3 eV) have to be used so far. Due to their small NT bandgaps these devices suffer from large off-currents. These leakage currents result from minority carrier

²For a single-wall NT in a typical device the bandgap is about 0.6 eV and for a metal Fermi energy located at the middle of the NT gap (at midgap line-up, cf. Fig. 14.1(b)) the SB is about 0.3 eV.

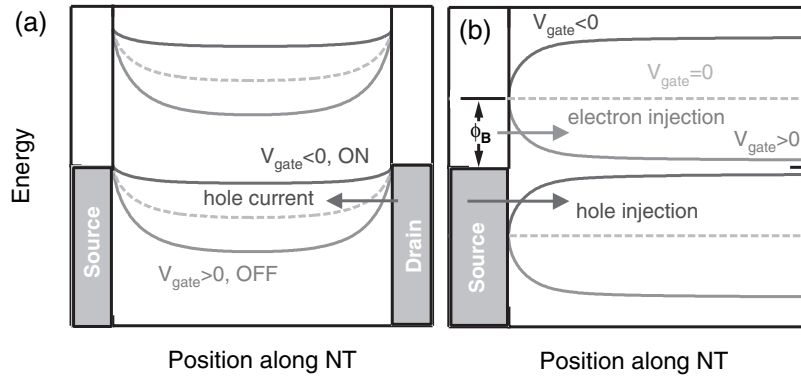


Fig. 14.1. (*Color online*) Working principle of (a) a conventional transistor with ohmic contact to the valence band and (b) a Schottky barrier transistor at midgap line-up of the metal Fermi energy with the semiconductor bands. The conventional transistor turns on at negative gate voltages due to the enhanced channel conduction. The SB transistor is ambipolar, i.e. it turns on at both negative and positive gate voltage due to the thinning of the SB width and thermally assisted tunneling.

injection at the drain contact and will be explained below based on the SB model of a CNFET. Another very promising route to create conventional FETs from a carbon nanotube is to dope both ends of the NT and use these ends as source and drain contacts [22]. This device setup prevents the formation of SBs and leads to transistor action from the modulation of the channel resistance. Subthreshold slopes close to the thermal limit and high on-currents have been observed in such devices [22]. Because of the required extended regions of doped NT it is not clear so far to which size these devices can be scaled down. Very recently, Lin et al. have used a double-gate device geometry to fabricate CNFETs with unipolar n- and p-type bulk switching and excellent performance in the subthreshold regime [23].

Due to the difficulty to achieve ohmic contacts to carbon nanotubes, a good understanding of the consequences and implications of SBs on the transport properties of CNFETs is necessary for further exploration of these promising devices. In addition, new optoelectronic applications are possible due to their existence [15, 24] and can be understood based on the transport model introduced in the following.

14.2.1 Needle-Like Contact Model

In order to study the operation principle of a SB-CNFET we begin with the idealized model of the CNFET shown in Fig. 14.2. We assume that the metal electrode is a cylinder with the same diameter as the NT forming a perfectly sharp needle-like contact to the NT. The gate electrode is a metal cylinder surrounding the contact. This device geometry is advantageous as

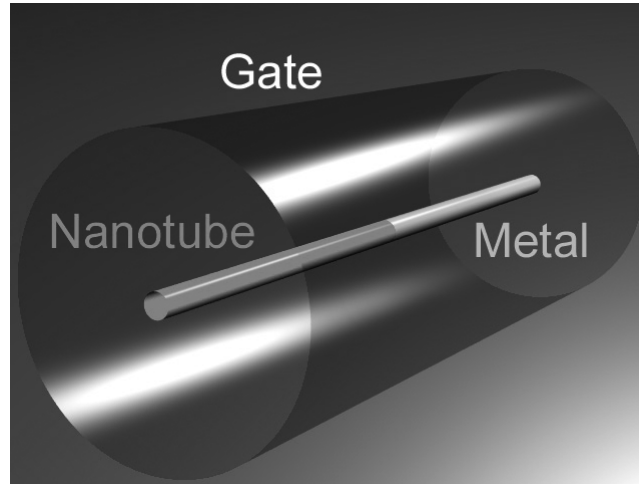


Fig. 14.2. (*Color online*) Geometry of the needle-like contact model. A cylindrical gate surrounds the nanotube-metal junction. The metal electrode consists of a cylinder of the same diameter as the NT, i.e. on the order of 1 nm.

the electrostatic kernel $G(z)$ is known analytically [25,26]. Thus for a given charge distribution $\rho(z)$ on the metal-nanotube junction we can evaluate the electrostatic potential $V(z)$ along the NT:

$$V(z) = V_g + \frac{R_g}{4\pi} \int G(z - z') \rho(z') dz', \quad (14.1)$$

where R_g is the gate radius and V_g is the applied gate voltage. We further assume that an electrostatic potential along the NT rigidly shifts the valence and conduction bands of the NT. Thus the local density of states (DOS) of the NT, $D(E)$ [27], is shifted and the charge on the NT can be found by integration over energy:

$$\rho(z) = -\frac{e}{\epsilon} \int_{E_c(z)}^{\infty} F(E) D(E - V(z)) dE + \frac{e}{\epsilon} f, \quad (14.2)$$

where $F(E)$ is the Fermi distribution and $E_c(z)$ is the local position of the conduction band. We have chosen the case where additional electrons populate the NT conduction band. The case for holes in the valence band is obtained analogously. The second term on the right hand side is added in order to take uniform doping into account. Here, f is the fraction of dopants per atom of the NT and ϵ is the dielectric constant of the surrounding oxide.

Equations (14.1) and (14.2) need to be solved self-consistently. Transport over the short length of the NTs used in CNFETs is ballistic [6, 7] and the current through the transistor is calculated from the Landauer-Büttiker formula:

$$I = \frac{4e}{h} \int T(E)[F(E) - F(E + eV_d)]dE, \quad (14.3)$$

where V_d is the drain voltage (assumed to be small) and $F(E)$ is the Fermi distribution. The transmission $T(E)$ through the SB is calculated within the WKB approximation:

$$\ln T(E) = -\frac{4}{3bV_\pi} \int_{z_i}^{z_f} (\Delta^2 - [E + eV(z)]^2)^{1/2} dz, \quad (14.4)$$

where $b = 0.144$ nm is the bond length, Δ is half the NT bandgap, and $V_\pi = 2.5$ eV is the tight-binding parameter. The integration is performed along the NT between the classical turning points z_i and z_f . For the calculations we used a NT with a bandgap of 0.6 eV corresponding to a diameter of 1.4 nm. We neglect screening on the NT as it is negligible for a quasi-1D wire [28]. For the dielectric constant ϵ we choose a value of 3.9 as for SiO₂.

For a midgap line-up of the metal Fermi level with the NT bands, the calculated conductance, displayed in Fig. 14.3, is symmetric with respect to the applied gate voltage V_g . At large gate voltages the SB is thinned down to a few nanometers due to the high electric field at the contact. The barrier then allows a significant electron tunneling current into the NT conduction band at positive gate voltages and hole tunneling into the valence band at negative gate voltages (cf. Fig. 14.1(b)). The gate voltage required to turn

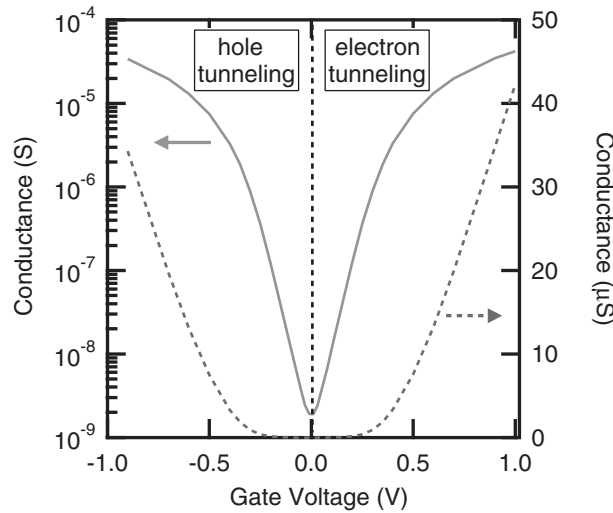


Fig. 14.3. (*Color online*) Calculated conductance as a function of the applied gate voltage for the needle-like contact and an oxide thickness of 50 nm. The Fermi energy of the metal is assumed to be at midgap of the NT bands. Solid red (*dashed blue*) curve is the conductance on a logarithmic (*linear*) scale.

the transistor from off ($V_g = 0$, low conductance) to on (high conductance) is about $V_g^{\text{on}} = 0.5$ V which is on the order of the bandgap (0.6 eV). The calculated transfer characteristic (I vs. V_g) is in good qualitative agreement with experimental data [9]. However, the turn-on gate voltage V_g^{on} is much smaller than in the experiment (typical values range from 1 to 20 V). This discrepancy is due to the ideal focusing of the electric field at the needle-like contact. In an actual device, planar gate geometries are used and we need to take this geometry explicitly into account for a realistic model of the transistor.

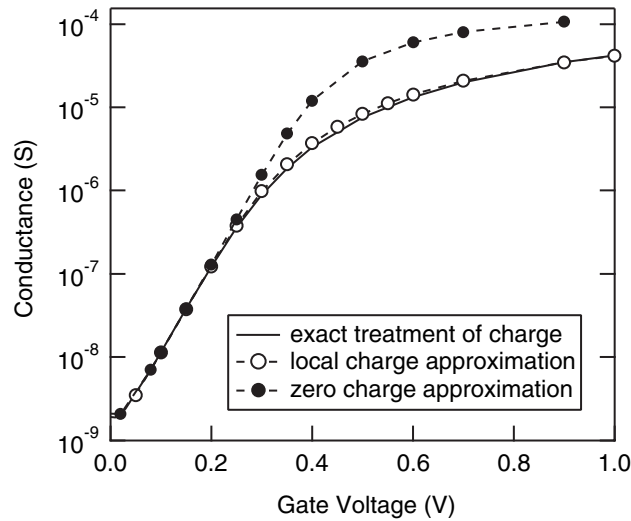


Fig. 14.4. Comparison of different approximations for the electrostatic potential caused by charge on the NT. All calculations are performed within the needle-like contact model.

It is instructive to compare various approximations for the description of the electrostatic potential resulting from charge on the NT. In Fig. 14.4 the calculated conductance within the needle-like contact model is displayed for the exact treatment and two approximations. In the turn-on regime up to about 0.3 V, charge on the NT can be completely neglected (see the zero-charge approximation in Fig. 14.4) because the barrier shape which controls the conductance is only weakly affected by charge while the bulk of the NT does not affect the conductance in this voltage regime. However, in the on-state the position of the bulk conduction band limits the current and the zero-charge approximation breaks down. A strictly local approximation, i.e. if we assume that the potential due to charge on the NT is given by $V_{\text{local}}(x) = U\rho(x)$, is valid even far beyond the turn-on regime because the potential in the bulk of the NT is modelled with sufficient accuracy.

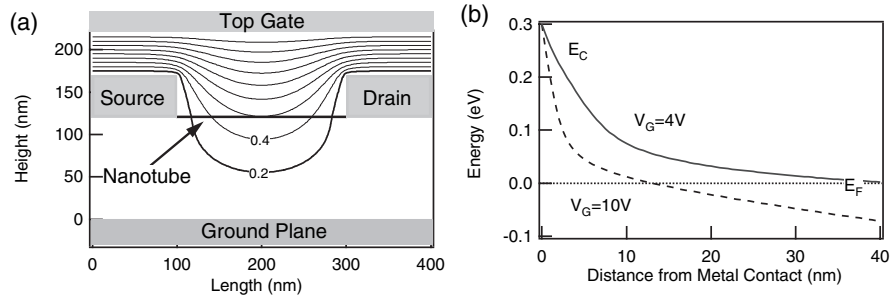


Fig. 14.5. (a) Cross-section through a carbon nanotube transistor with planar gates. For a top gate device the gate voltage is applied to the top electrode while the bottom electrode is grounded. Potential contour lines in steps of 0.2 V are shown for $V_g = +2$ V. (b) Calculated conduction band along the NT at midgap line-up for $V_g = +4$ V (solid line) and $V_g = +10$ V (dashed line). The resulting conductance is displayed in Fig. 14.6 ($t_{\text{ox}} = 100$ nm).

14.2.2 Influence of the Contact Geometry

To obtain a better understanding of the experimentally observed transport characteristics the carbon nanotube transistor has to be explored within a planar geometry displayed in Fig. 14.5(a). The gate voltage is applied to a top gate as in [4] and a grounded bottom electrode has been added for a convenient electrostatic calculation. The source and drain contacts possess a finite thickness in our device. The two-dimensional electrostatic boundary problem can be solved by standard techniques and we treat the potential due to charge on the NT in a local approximation. This is sufficiently accurate even beyond the turn-on regime as we have demonstrated within the needle-like contact model (see Fig. 14.4). We focus on a midgap line-up. The band bending for two gate voltages is shown in Fig. 14.5(b). At $V_g = 4$ V there is already considerable charge on the NT, however, the SB at the contact is still about 10 nm wide at 0.1 eV above the Fermi energy. Consequently, the tunneling probability and the current are negligible. With a very large gate voltage of $V_g \geq 10$ V, it is possible to thin down the SB to a few nanometers sufficient for considerable injection of electrons.

In Fig. 14.6 the conductance is plotted versus gate voltage for several top gate devices with varying oxide thickness and contact geometries. (Due to the symmetric form of the curves only positive gate voltages are considered, i.e. transport due to electron injection.) The shape of the conductance curves is similar to the needle-like contact, however, much larger gate voltages are required to turn on the transistors. As the oxide thickness is reduced a steady increase of the device performance, i.e. turn-on at lower gate voltage, can be observed. The crucial importance of the contact geometry for a SB-CNFET becomes apparent when the thickness of the source and drain contacts is reduced from 50 nm to 5 nm keeping all other parameters, in particular the

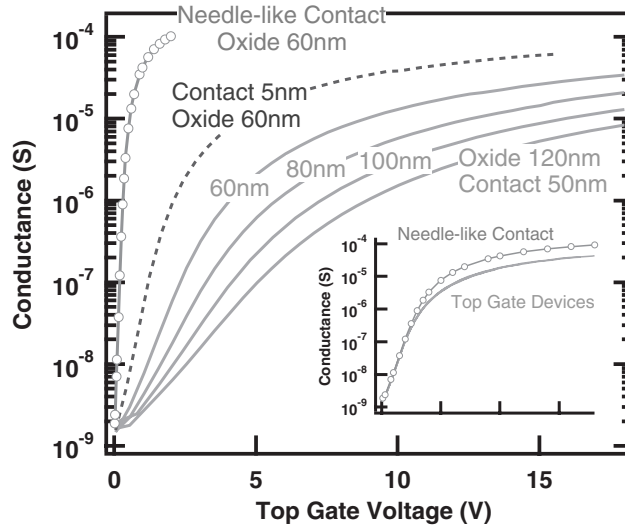


Fig. 14.6. (*Color online*) Calculated conductance versus gate voltage for top gate devices (device geometry as in Fig. 14.5(a)) with various gate oxide thicknesses (i.e. nanotube-top gate distance) and contact thickness of 50 nm (*solid blue lines*) and 5 nm (*dashed blue line*). The needle-like contact model is included for comparison (*solid red line*). The inset shows that the conductance of all top gate devices can be scaled to a single curve.

oxide thickness, fixed. Due to the sharper edge of the source contact a larger electric field can be achieved at a given top gate voltage and the device turns on at lower gate voltage. This is in contrast to a conventional transistor which turns on due to the modulation of charge carriers in the channel. For the needle-like contact geometry the improvement due to field focusing at the contact is dramatic as shown in Fig. 14.6. Thus the contact plays a key role for the transport characteristics of a SB-CNFET. Its precise control is crucial to fabricate devices with excellent and reproducible performance.

The transport curves for top gate devices can be scaled to a single functional form as demonstrated in the inset of Fig. 14.6. Even the conductance of the needle-like contact CNFET with a very different geometry can be scaled onto the other curves within the turn-on regime. In conclusion, the main effect of a specific contact geometry is to scale the gate voltage range. A quantitative study of scaling issues will be given in Sect. 14.2.4. Here we note that for problems which require an accurate treatment of the potential from charge on the NT, e.g. to include dopants on the NT or dipoles at the NT-metal contact, the idealized needle-like contact model is more appropriate. A comparison with experiments is obtained by scaling the gate voltage range.

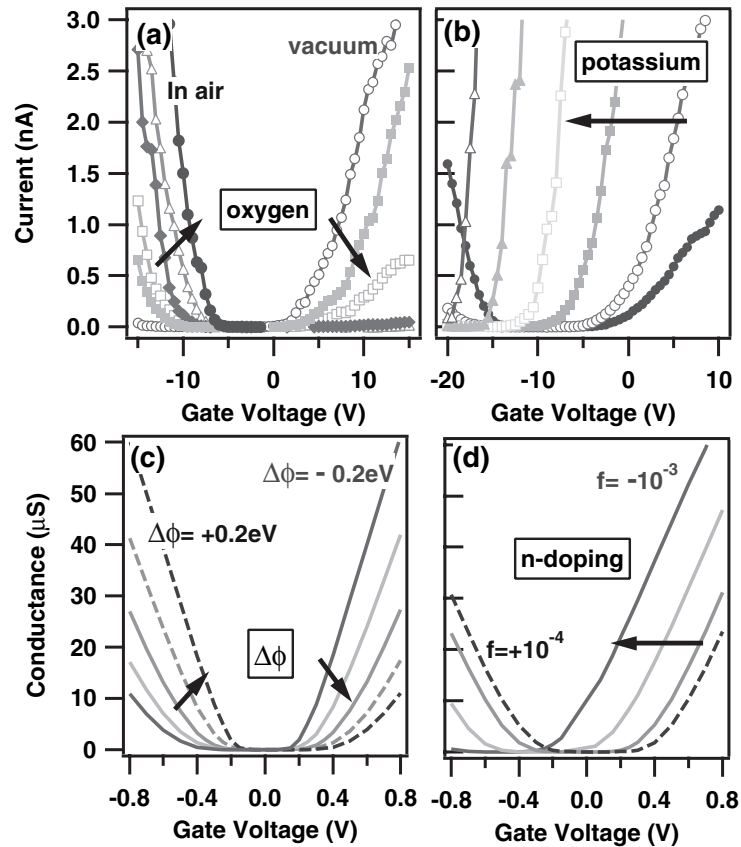


Fig. 14.7. (*Color online*) Effect of gas adsorption and doping on a SB-CNFET. (a) and (b) are experimental data and (c) and (d) calculations within the needle-like contact model. In (a) the vacuum annealed (n-type) FET (red, open circles) has been exposed to increasing amounts of oxygen until the ambient is reached (blue, filled circles). In (b) the curves from right to left correspond to increasing deposited amounts of potassium. In (c) the work function difference $\Delta\phi$ between metal and NT is changed from -0.2 eV (solid red line) to $+0.2\text{ eV}$ (dashed blue line) in steps of $+0.1\text{ eV}$. In (d) the doping atomic fraction is from left to right n-type 10^{-3} (red), 5×10^{-4} (orange), and 10^{-4} (green), and p-type 10^{-4} (dashed blue line), respectively. More details can be found in [11] and [18].

14.2.3 Effect of Gas Adsorption

A longstanding puzzle has been the effect of gas adsorption on the nanotube electronic structure. It has been proposed that e.g. oxygen adsorption leads to doping of the nanotube [29, 30]. However, as shown in Fig. 14.7(a), the effect of oxygen on the transport properties of a CNFET is a reversible transition from p-type (devices prepared in air) to n-type after annealing the transistor

in vacuum [18]. In contrast, the deposition of an n-type dopant atom such as potassium, Fig. 14.7(b), shifts the transfer characteristics with respect to the gate voltage. It is known that the work function of a metal surface is altered significantly upon the adsorption of gases due to the formation of interface dipoles. Thus the local work function of the metal electrode can be modified considerably by the adsorption of oxygen at the contacts. If the work function of the metal electrode changes the line-up of the metal Fermi energy with the NT bands will shift [17]. (Note that this is unique for the contact between a metal and a nanotube. In a conventional, planar semiconductor device the position of the Fermi energy is pinned by metal-induced gap states [16].)

Within the needle-like contact model it is straight forward to compare the effect of doping with that of a shift in the line-up, i.e. a reduction of the SB height to the conduction band and an increase of the SB height to the valence band or vice versa. The results of such calculations are shown in Figs. 14.7(c) and (d). Apart from the gate voltage scale there is a compelling agreement between the calculation and the experimental data. While n-type doping shifts the transport curves to more negative gate voltages, a change in the work function promotes either the p- or the n-type branch of conduction and reduces the other but the minimum conductance occurs at zero gate voltage for all line-ups.

The characteristic modifications of the conductance in the two cases can be explained based on the band bending at the NT-metal contact. Figure 14.8(a) shows the diagram for an increased metal work function. In this case, a lower SB forms to the valence band of the NT than to the conduction band. At zero gate voltage, there is a negligibly small current due to

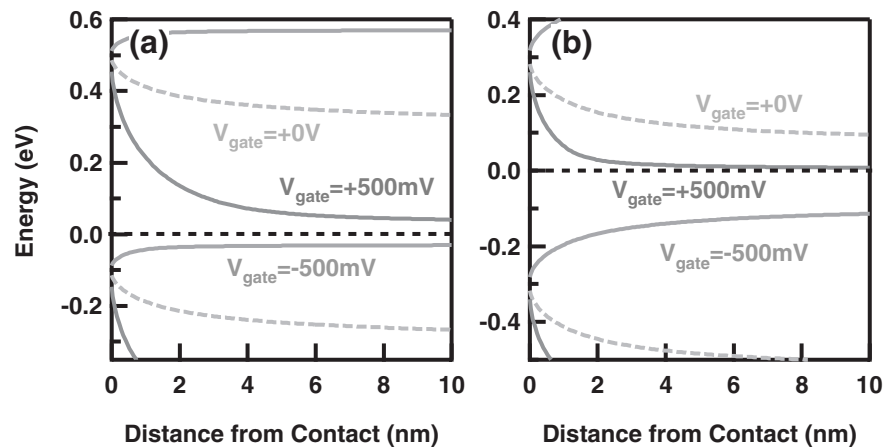


Fig. 14.8. (*Color online*) Calculated NT band bending at gate voltages of $V_g = +500$ mV, 0 mV, and -500 mV in the case of (a) a metal work function increase of $\Delta\phi = +0.2$ eV and (b) n-type uniform doping of the NT with a fraction of 5×10^{-4} .

thermionic emission into the valence band. Its magnitude is equal to the off-conductance for a midgap line-up as the thermal barrier is still half the NT bandgap, i.e. 0.3 eV in our calculation. Thus there is no change of the conductance at $V_g = 0$ (cf. Fig. 14.7(c)). When a negative gate voltage is applied the conductance increases exponentially due to a thermal hole current above the reduced barrier to the valence band. At larger negative gate voltages holes can also tunnel into the NT valence band. However, the SB for electrons is much larger in this case than for a midgap line-up which lowers the tunneling probability according to (14.4). The achievable conductance at positive gate voltages due to electron tunneling is thus reduced (see Fig. 14.7(c)).

For a uniformly n-type doped NT at midgap line-up, as shown in Fig. 14.8(b) for comparison, there is a considerable band bending even at zero gate voltage and correspondingly the conductance increases compared to an undoped NT (Fig. 14.7(d)). Upon a positive gate voltage the SB to the conduction band can be further thinned and electron tunneling is promoted. However, larger negative gate voltages are needed compared to the undoped NT to achieve the same band bending of the valence band and accordingly for the same amount of hole current. Hence the entire conductance curve shifts to the left upon n-type doping and analogously to the right for p-type doping.

The change of the local work function difference between a metal electrode and a carbon nanotube that we have assumed above has been observed directly in experiments by scanning probe methods [31]. Because the work function depends sensitively on the local environment one cannot simply take the metal and nanotube work function from a textbook and compute the band line-up. Instead, a microscopic picture of the creation of oxygen dipoles and the charge rearrangement at the interface is crucial for a quantitative understanding [31].

The controlled transition from p- to n-type transistors by gas adsorption and doping has been used to fabricate the first logic gates from single carbon nanotubes [8]. Figure 14.9(a) shows the device geometry of an inverter created from a single carbon nanotube which lies above three metal contacts. After the first preparation step in air both transistors display p-type transport. The right CNFET was then protected by a photo resist and subsequent potassium doping turned only the unprotected device to an n-type FET. By applying the in-voltage to the common back gate of the two CNFETs and taking the out-voltage at the central metal contact the device operates as a voltage inverter (see Fig. 14.9(b) for a sketch of the electronic circuit). The measured device characteristic, Fig. 14.9(c), demonstrates the voltage inversion and the achievement of a voltage gain, i.e. a ratio of output to input voltage larger than one. This is an essential prerequisite to use a logic gate in a real circuit consisting of many gates.

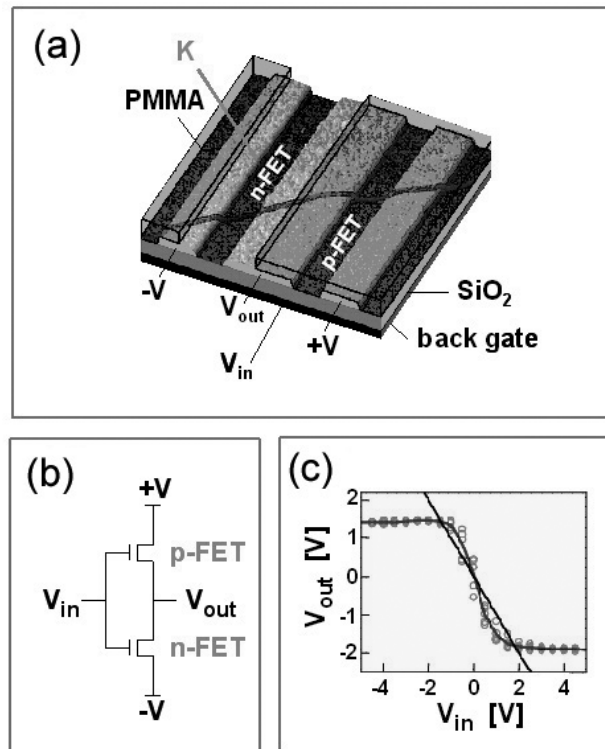


Fig. 14.9. (*Color online*) Inverter created from a single carbon nanotube [8]. (a) shows a 3D SEM image of the device in which the blue line marks the single-wall carbon nanotube. Three metal electrodes contact the carbon nanotube creating two transistors. The right transistor is protected by a resist (PMMA, shown by transparent *blue boxes*) from potassium (**K**) doping and remains p-type (as prepared in air) while the left changes to n-type upon doping. The bias voltage is applied to the outer metal contacts while the out-voltage is taken from the central contact. The in-voltage is applied to the back gate. (b) is a schematic plot of the electronic circuit of an inverter created from an n- and p-type FET. In (c) the measured voltage characteristic of the carbon nanotube inverter is displayed.

14.2.4 Scaling of the SB-CNFET Performance

In the last sections, we have demonstrated that the SB model explains transistor action in CNFETs and solves the puzzle of gas adsorption. We concluded that the contact geometry plays a key role for turn-on performance at low bias voltage. In this section we consider the consequences of operation as a SB transistor for device performance, in particular the scaling with reduced device size. An understanding of the scaling relations is a basic ingredient to judge the technological potential of carbon nanotube transistors.

The first extrapolation of the performance [13] has been based on CNFETs with fairly thick (bottom) oxides (≥ 20 nm). From that data it seemed that a subthreshold slope, $S = (d \log I / dV_g)^{-1}$ [32], below 100 meV/decade should be possible at ultra-thin oxides between 5 and 2 nm. Surprisingly, the actual devices did not fulfill this prediction. Instead a levelling off of S at low oxide thickness was observed [14].

To study the turn-on performance we need to extend our model to finite drain voltages. At finite bias voltage, a Fermi energy cannot be defined for the NT anymore and a non-equilibrium model such as the Greens function method described in [33] (or in Chaps. 4 to 6) must in principle be applied. Therefore, it may seem surprising at first that an adequate model of the turn-on regime, i.e. as the device is turned from the off-state (low current) to the on-state (high current), can be developed neglecting charge on the NT as shown below. The key observation is that the current is limited by the transmission through the SB and thus by the electrostatic potential in the vicinity of the contact. The main effect of charge on the NT, in contrast, is to change the electrostatic potential within the channel. In the turn-on regime, the channel limits the current only when there is negligible charge on the NT. (In that case the current is due to thermionic emission and not tunneling.) Therefore, we can neglect charge on the NT if we are interested only in the current through the device in the off-state and turn-on regime. However, in the on-state, i.e. as the SB becomes transparent, the non-equilibrium charge on the NT and the capacitance of the gate to NT may become important for the magnitude of the on-current and cannot be neglected [34].

Neglecting charge on the NT simplifies the electrostatics significantly. In particular, we can reduce the problem to solving the Laplace equation in two

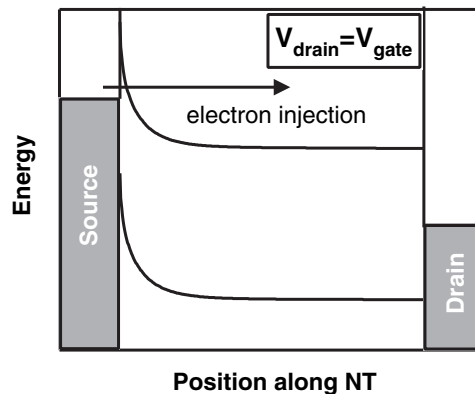


Fig. 14.10. Band diagram of a SB-CNFET in the regime of current saturation, i.e. if drain and gate voltage are equal (the source is held at zero potential). All electrons injected at the source can be collected at the drain contact where they face no potential barrier.

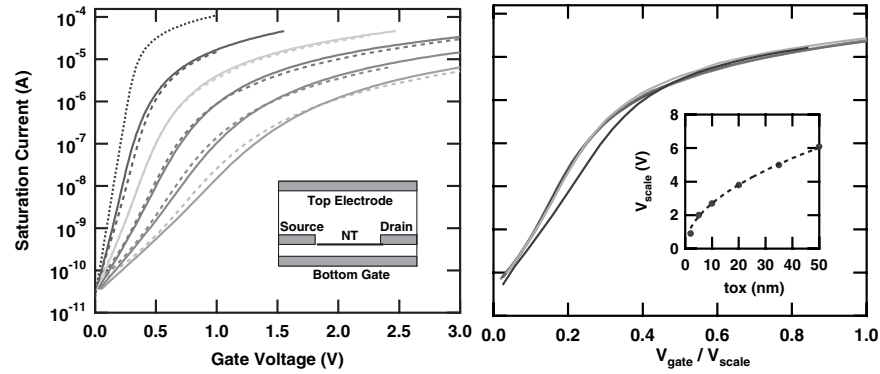


Fig. 14.11. (*Color online*) Calculated transfer characteristics for bottom gate SB-CNFETs at midgap with varied oxide thickness. Left panel shows the full calculations (*solid lines*) for $t_{\text{ox}} = 35, 20, 10, 5$ and 2 nm, from right to left and the thermal limit (*dotted black line*). The *dashed lines* are calculations with the analytic model described in the text. The inset displays the bottom gate geometry used in the calculation. The right panel demonstrates the scaling of all curves to a single unique function except for the ultra-thin 2 nm oxide. In the inset the extracted scaling voltage has been plotted versus oxide thickness. A square-root fit is indicated by the dashed line in the inset.

dimensions fixing the boundary conditions by the given drain and gate voltage [35]. From the electrostatic potential we can calculate the transmission and the current as in the previous sections. The electronic structure of the NT is treated as before.

For the calculation we choose the regime of current saturation, i.e. $V_d = V_g$ shown in Fig. 14.10, where the barrier at the drain contact vanishes. In this case there is only a voltage drop and an electric field at the source contact held at $V_s = 0$. Thus all charge carriers injected at the source are collected at the drain and the current saturates. The scaling relations of the turn-on performance are unaffected by this choice. Experimentally the independence of the subthreshold slope on the applied drain voltage has been confirmed [13, 14]. We use the saturation regime in the following to derive an analytic model and to give explicit scaling relations for the turn-on performance.

The left panel of Fig. 14.11 displays the results obtained for bottom gate CNFETs with different oxide thicknesses t_{ox} . A continuous improvement of the subthreshold slope with decreasing t_{ox} is observed. However, even for an ultra-thin oxide of 2 nm and with an ideal sharp corner contact as in our calculation, the thermal limit of a conventional transistor is not reached. In a similar way as in the low bias voltage limit (cf. Fig. 14.6) we can scale the gate voltage for every device from the left panel of Fig. 14.11 to find a single functional form of the saturation current, shown in the right panel. Deviations are seen only for $t_{\text{ox}} = 2$ nm. The extracted scaling gate voltages

which are a measure of the required turn-on voltage are plotted in the inset of the right panel of Fig. 14.11 as a function of t_{ox} . A square-root fit (dashed line in the inset) gives an excellent description.

In order to understand whether the square root behavior of the turn-on voltage is of general validity we consider a simple analytic model. Note, that only the electrostatic potential close to the source (metal) contact is needed to evaluate the saturation current. While there is no analytic solution in the bottom gate device geometry, we can solve the electrostatic boundary problem for a device with two planar gates both at a distance t_{ox} from an infinitely thin sheet contact [36]. The potential as a function of distance z from the contact is $V(z) = 2V_g\pi^{-1/2}(z/t_{\text{ox}})^{1/2}$. In the thick oxide limit we can further replace the lower integration boundary, $\Delta - eV_d$, by $-\infty$. We can directly insert the potential into (14.3) and (14.4) and solve for the saturation current:

$$I_{\text{sat}} = \frac{4e\Delta}{h} H\left(\frac{V_g}{V_{\text{scale}}^{\text{dg}}}, \frac{\Delta}{kT}\right), \quad (14.5)$$

where $H(x, y)$ is

$$H(x, y) = \int_{-\infty}^{\infty} \frac{\exp(-h(s)/x^2)}{1 + \exp(sy)} ds \quad (14.6)$$

and $h(s)$ is

$$h(s) = \int_{\max(0, -1-s)}^{1-s} t[1 - (s+t)^2]^{1/2} dt. \quad (14.7)$$

The ‘‘scaling voltage’’ for this double-gate device is

$$V_{\text{scale}}^{\text{dg}} = \left(\frac{2\pi\Delta^3}{3be^2V_\pi}\right)^{1/2} t_{\text{ox}}^{1/2}. \quad (14.8)$$

Since the saturation current depends only on $V_g/V_{\text{scale}}^{\text{dg}}$ a change of t_{ox} leads merely to a scaling of the gate voltage. With a single empirical parameter we can use this idealized model to reproduce the results for the bottom gate devices. If we choose the scaling voltage for the bottom gate geometry as $V_{\text{scale}}^{\text{bg}} = 2.2V_{\text{scale}}^{\text{dg}}$ the saturation current can be calculated for all t_{ox} as shown in the left panel of Fig. 14.11 by dashed lines. An excellent agreement is achieved within the whole range of oxide thicknesses. Thus the scaling with t_{ox} of the ideal double gate device applies also for the bottom gate device.

From (14.8) we conclude that the turn-on voltage scales as the square-root of the oxide thickness which is in agreement with our previous empirical finding. By differentiating the saturation current with respect to the gate voltage we obtain the subthreshold slope:

$$S = \left(\frac{d \log I_{\text{sat}}}{dV_g}\right)^{-1} = V_{\text{scale}} F\left(\frac{V_g}{V_{\text{scale}}^{\text{dg}}}, \frac{\Delta}{kT}\right) \quad (14.9)$$

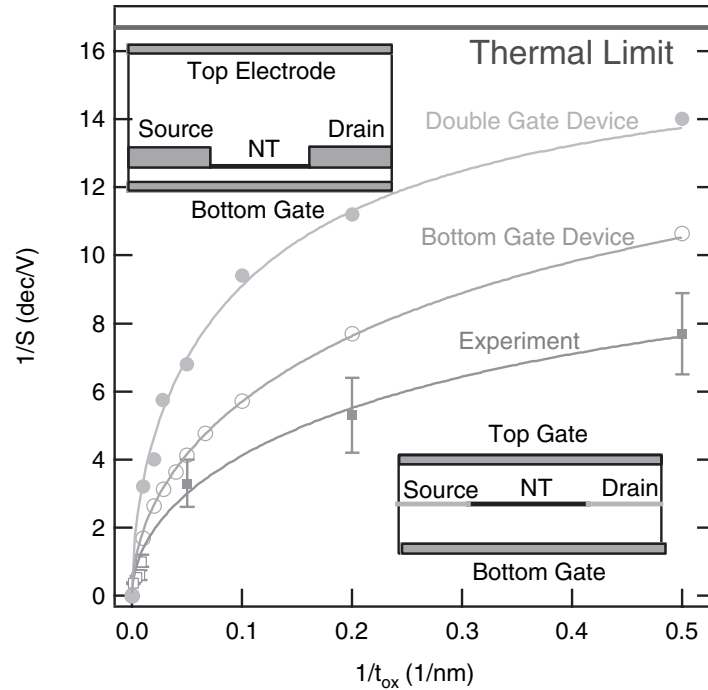


Fig. 14.12. (*Color online*) Inverse subthreshold slope S as a function of the inverse oxide thickness t_{ox} . Solid curves are fitted as described in text. Bottom red curve is experiment – open red squares are data from previous work, filled red squares are from our work [14]. Data at $t_{\text{ox}} = 2$ nm and 5 nm represent averages over several devices. For $t_{\text{ox}} = 20$ nm our result agrees with previous reports [4]. Upper two curves are calculated for $V_d = V_g$. The upper left inset shows the bottom gate device geometry (*open green circles*) while the lower right inset shows the double gate device (*filled orange circles*).

where

$$F(x, y) = \ln 10 \frac{H(x, y)}{\partial H(x, y) / \partial x}. \quad (14.10)$$

The subthreshold slope is evaluated at its minimum value in the turn-on regime, i.e. at a fixed V_g/V_{scale} . Thus the subthreshold slope scales as V_{scale} which is as the square-root of t_{ox} .

In Fig. 14.12 the inverse subthreshold slope is plotted versus the inverse oxide thickness. For the experimental data a levelling off is seen as the oxide thickness decreases. The performance does not approach the thermal limit of a conventional transistor, a value of about 60 meV/decade. Results for calculated bottom gate devices show a very similar qualitative behavior, however, at lower values of S , i.e. better performance. (The better performance for the calculated devices is probably due to the sharper contact geometry. Ex-

perimentally, the contact geometry cannot be characterized accurately on the nanometer scale.) The crucial impact of the contact geometry on device performance is emphasized by a calculation for a planar double gate device with contacts that are only as thick as the NT diameter, i.e. 1.4 nm. The dependence of the subthreshold slope on t_{ox} shows a similar functional form, however, at significantly enhanced performance. For infinitely thin oxides, the subthreshold slope must saturate at the thermal limit. We can thus use a fitting function $S = [\alpha t_{\text{ox}} + (kT \ln 10)^2]^{1/2}$, with α a fitting parameter which depends on the specific contact geometry. Both the experiment and the calculations in the two device geometries can be fitted with this interpolation function as shown in Fig. 14.12.

From our scaling analysis we conclude that a precise control of the NT-metal contact geometry is essential for SB-CNFETs with high turn-on performance and reproducible properties. The creation of a sharp contact geometry can be much more effective for superior performance than reducing the oxide thickness for a given device design.

For a conventional transistor the subthreshold slope decreases linearly at low temperatures. However, from (14.9) we find a decrease which levels off to a non-vanishing value at zero temperature as shown in Fig. 14.13. This unusual

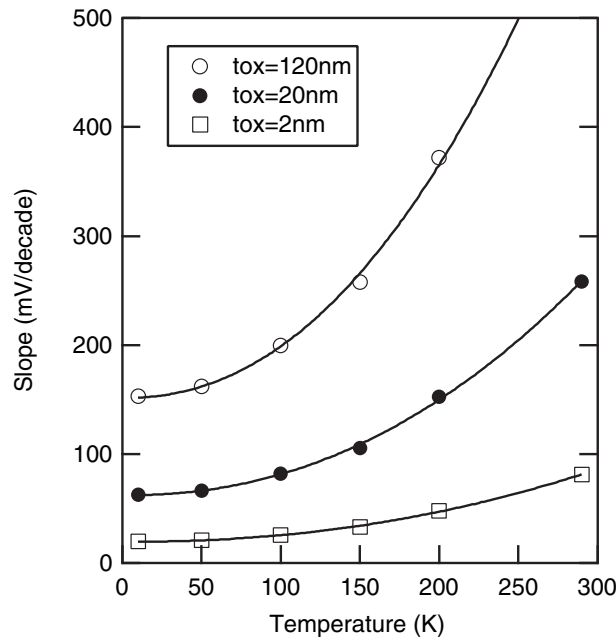


Fig. 14.13. Calculated temperature dependence of the subthreshold slope for bottom gate devices with oxide thicknesses of $t_{\text{ox}} = 2, 20,$ and 120 nm. This temperature dependence is in good agreement with experimental data [13].

low temperature behavior of S has been observed experimentally [13] and provides an experimental way to distinguish a SB-CNFET from a CNFET with ohmic contacts. The evaluation of the temperature dependence of S can also be used to determine the height of the SB in a given device [37].

14.2.5 Scaling of the Drain Voltage

The scaling relations for the turn-on performance of a SB-CNFET have important consequences for the operation of such devices, especially when ultra-thin gate oxides are used. Because the turn-on voltage decreases as the square-root of t_{ox} it is below 1 V for an oxide thickness of 5 nm. This voltage is comparable to typically applied drain voltages in the operation regime of a transistor. Both the SB at the source and at the drain contact are therefore affected and charge carriers can be injected at both contacts at the same time.

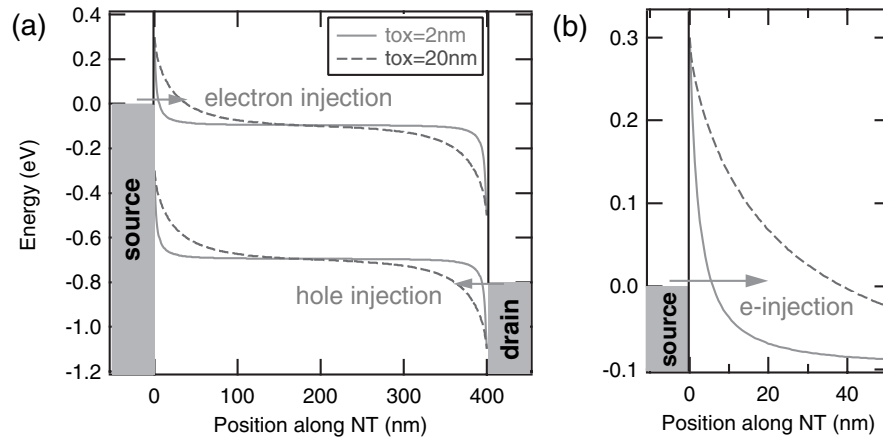


Fig. 14.14. (*Color online*) Band diagrams for midgap SB-CNFETs with $t_{\text{ox}} = 2$ nm and 20 nm for a symmetric potential drop at source and drain contacts, i.e. for $V_g = V_d/2 = 0.4$ V (transistor off-state). (a) shows the bands for the full length of the device with arrows indicating tunneling of electrons at the source and tunneling of holes at the drain contact. (b) gives a close-up view at the source contact. Note, that the SB is too wide for the device with $t_{\text{ox}} = 20$ nm to allow a significant tunneling current.

In a typical experiment, the source contact is held at zero potential and the bias (drain) voltage is applied to the drain contact. In this case there is a voltage drop of V_g at the source contact and of $V_g - V_d$ at the drain contact. Figure 14.14(a) displays the situation of a symmetric potential drop at the source and drain contact, i.e. for $V_g = V_d/2$, and for midgap SB-CNFETs with oxide thicknesses of 20 nm and 2 nm. At the source contact, electrons

can be injected into the NT conduction band while holes can tunnel into the valence band from the drain contact. For an oxide thickness of 20 nm, however, the barriers are very wide at the contacts and the tunneling current is negligibly small (see Fig. 14.14(b)). For an ultra-thin oxide of 2 nm, on the other hand, the barriers are only a few nanometers wide and a significant current flows which consists of equal electron and hole contributions injected at the source and drain contact, respectively.

A symmetric potential drop at source and drain contact as in Fig. 14.14(a) corresponds to the minimum device current (the off-state of the transistor) for a given drain voltage. The full transfer characteristics (I vs. V_g) are shown in Fig. 14.15(a) to (d) for both devices at positive and negative drain voltages. A midgap line-up has been assumed which leads to symmetric, ambipolar transport curves. The right branch of the transfer characteristics is dominated by electron injection while the left branch results from hole injection. In Fig. 14.15(a) the electron and hole current have been included explicitly for $V_d = -0.8$ V. At the minimum of the total current there are equal hole and electron contributions. At general gate voltages, either holes or electrons dominate the current and we can consider the other type as minority charge carriers.

In Fig. 14.15 we observe a shift of the minimum current with V_d according to the relation $V_g^{\min} = V_d/2$. (Thus at negative V_d , (a) and (c), the curves shift to the left with increased $|V_d|$, and at positive V_d , (b) and (d), they shift to the right.) In addition, the off-current increases with V_d . For the CNFET with a moderate oxide thickness of 20 nm, Fig. 14.15(c) and (d), the change of the transfer curves with V_d is rather small up to $V_d = 0.8$ V and there is only a small increase of the off-current. However, for a device with an ultra-thin oxide ($t_{\text{ox}} = 2$ nm, Fig. 14.15(a) and (b)) the turn-on voltage is much smaller and thus the increase of the off-current is dramatic. Even at a low drain voltage of $V_d = 0.4$ V the on/off ratio, $I^{\text{on}}/I^{\text{off}}$, is only three orders of magnitude and at larger drain voltages the device becomes inoperable as a transistor due to the decreasing on/off ratio. The calculated transfer characteristics displayed in Fig. 14.15 are in excellent agreement with experimental data. Both the shift of the transport curves with drain voltage and the exponential increase of the off-current have been confirmed experimentally [38].

We can apply the analytic model introduced in the previous section for the saturation current to calculate the off-current and derive explicit scaling relations with t_{ox} and V_d . From a comparison of the band diagrams in Fig. 14.14(a) and Fig. 14.10 we observe that the electron and the hole currents in the off-state correspond to the saturation current at a voltage of $V_g = V_d/2$. The off-current which consists of an equal hole and electron current is then given by:

$$I^{\text{off}}(V_d) = 2 I_{\text{sat}}(V_g = V_d/2), \quad (14.11)$$

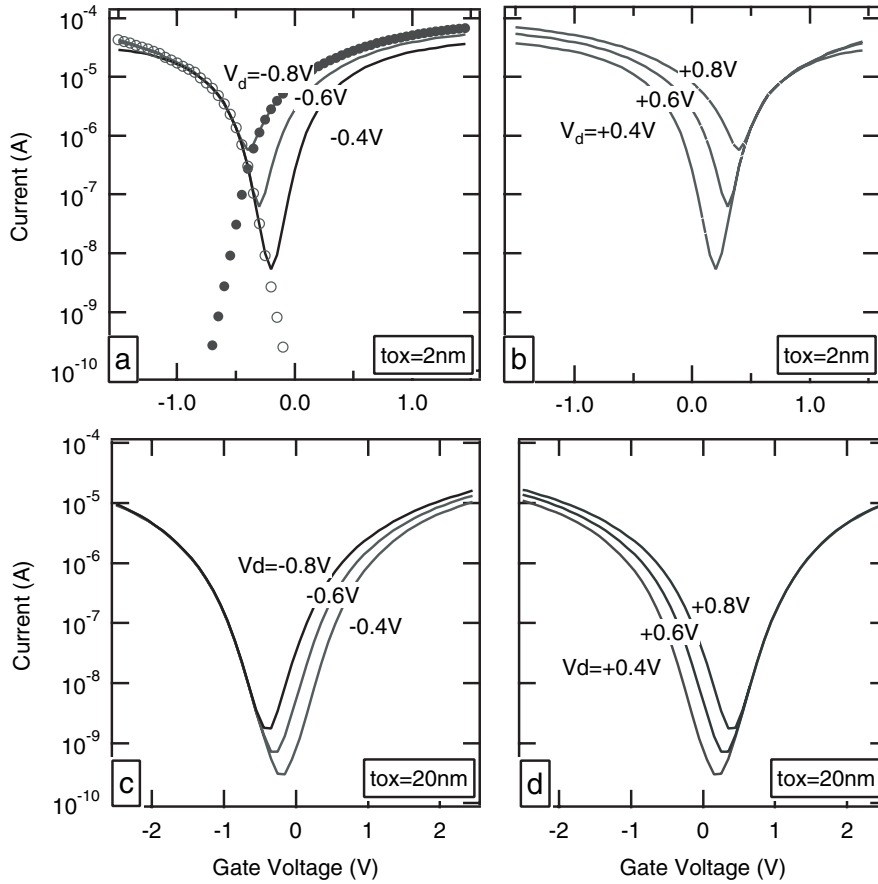


Fig. 14.15. Calculated transfer characteristics (I vs. V_g) at positive and negative drain voltages. (a) and (b) show the case of a bottom oxide of $t_{\text{ox}} = 2$ nm and (c) and (d) the case of $t_{\text{ox}} = 20$ nm. In (a) the filled and open circles denote the electron and hole contribution to the current for $V_d = -0.8$ V, respectively.

and we can use (14.5) to analyze the scaling of the off-current. From (14.11) and the right panel of Fig. 14.11 it is apparent that the off-current must also increase exponentially with the applied drain voltage.

In Fig. 14.16 we have plotted the off-current as a function of the applied drain voltage for bottom gate CNFETs with $t_{\text{ox}} = 2$ and 20 nm, respectively. If we require a minimum on/off ratio for the transistor we obtain a square-root scaling as t_{ox} for the maximum allowed drain voltage. Numerically, we have determined the maximum drain voltage V_d for an on/off ratio of 10^4 or better and typical NT bandgaps ($0.3 \text{ eV} \leq E_g \leq 1.2 \text{ eV}$) to $V_d \sim \{(E_g[\text{eV}])^{1.3} - 0.2\} \sqrt{t_{\text{ox}}[\text{nm}]} \text{ V}$ for the simulated bottom-gate devices with midgap line-up. For CNFETs with ultra-thin oxides this constraint

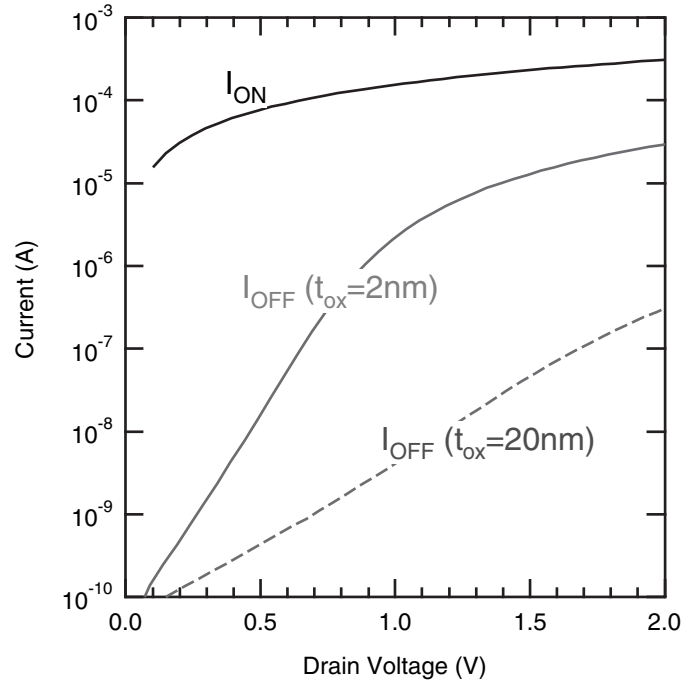


Fig. 14.16. (*Color online*) Calculated off-currents ($V_g = V_d/2$) versus drain voltage for oxide thicknesses of 2 nm (*solid red curve*) and 20 nm (*dashed blue curve*). The on-current (*black line*) depends linearly on the drain voltage.

limits the achievable on-current as it is proportional to the maximum drain voltage. Using NTs with larger bandgaps, i.e. smaller diameters, is one obvious option to achieve higher drain voltages.

The injection of minority charge carriers limits the device performance. It is important to note that the effect is present even for CNFETs with (nearly) ohmic contacts [6, 39] and can be large if the bandgap of the NT is small, i.e. up to about 0.4 eV. If there is an ohmic contact e.g. to the valence band there will be a SB with a height of the bandgap to the conduction band. Thus for a device with an ultra-thin oxide, which is required for high performance, there will be electron tunneling into the conduction band in the off-state. This limits the minimum off-current in the same way as for a midgap ambipolar CNFET.

A possible way to solve this problem is to fabricate a device with an asymmetric gating of the source and drain contact, e.g. by a variation of the oxide thickness [39, 40]. Such a device geometry allows to suppress the injection of minority charge carriers at the drain contact. Consequently, there is no exponential increase of the off-current with drain voltage. In addition, an asymmetric SB-CNFET can be operated either as an p- or n-type transistor

with the same (excellent) performance which is determined by the source contact geometry [39].

14.2.6 Light-Emission from a SB-CNFET

While the injection of minority charge carriers at the drain contact can make a CNFET inoperable as a transistor it allows to inject holes and electrons into the NT at the same time. By operating the CNFET in the off-state, i.e. choosing the gate and drain voltages according to $V_g = V_d/2$, we can achieve equal amounts of hole and electron current in the nanotube as shown in Fig. 14.14(a). If the applied drain voltage is chosen above the turn-on voltage of the transistor high electron and hole currents (exactly half of the off-current shown in Fig. 14.16) are achieved. Electrons which are injected at the source contact can recombine with holes injected at the drain contact with the emission of a photon. This is illustrated in Fig. 14.17(a). Experimentally, Misewich et al. have recently demonstrated that biasing a CNFET in the off-state indeed leads to the emission of polarized infra-red light [15].

Within our transport model of a SB-CNFET we can calculate the observed bias and gate voltage dependence of light emission from a NT if we assume an energy independent recombination probability. Figure 14.18 shows a calculation for a CNFET with an ultra-thin oxide of $t_{\text{ox}} = 2$ nm. (The transport characteristics of this device are given in Figs. 14.15 and 14.16.) We assume two different models for the recombination of electrons and holes with emission of a photon. The first is efficient recombination, i.e. every electron-hole pair leads to the emission of a photon, and the number of emitted photons is proportional to the minimum of the hole and electron current.

For inefficient recombination, on the other hand, there is only a finite (small) probability of an electron and a hole to recombine under photon emission. In that case the number of photons is proportional to the number of electrons (the electron current) and the number of recombination attempts (given by the number of holes, i.e. the hole current). Thus the number of emitted photons is proportional to the product of hole and electron current.

Both models lead to an exponential increase of the number of emitted photons with applied drain voltage (at the maximum value for $V_g = V_d/2$). This follows naturally from the variation of the off-current because the voltage requirement for maximum light emission is identical to the off-state. Thus the maximum number of photons is proportional to $I^{\text{off}}(V_d)$ or $[I^{\text{off}}(V_d)]^2$ for efficient or inefficient recombination, respectively. Consequently, Fig. 14.16 can be viewed as the drain voltage dependence of the maximum photon emission from a CNFET. The SB transport model of the CNFET describes the gate and drain voltage dependence of light emission well and can be used to guide the scaling of these optoelectronic devices. However, it cannot be used to determine which mechanism of electron-hole recombination prevails [15].

Recently, the recombination yield per electron-hole pair has been determined to 10^{-6} to 10^{-7} depending on NT length by measurements of the

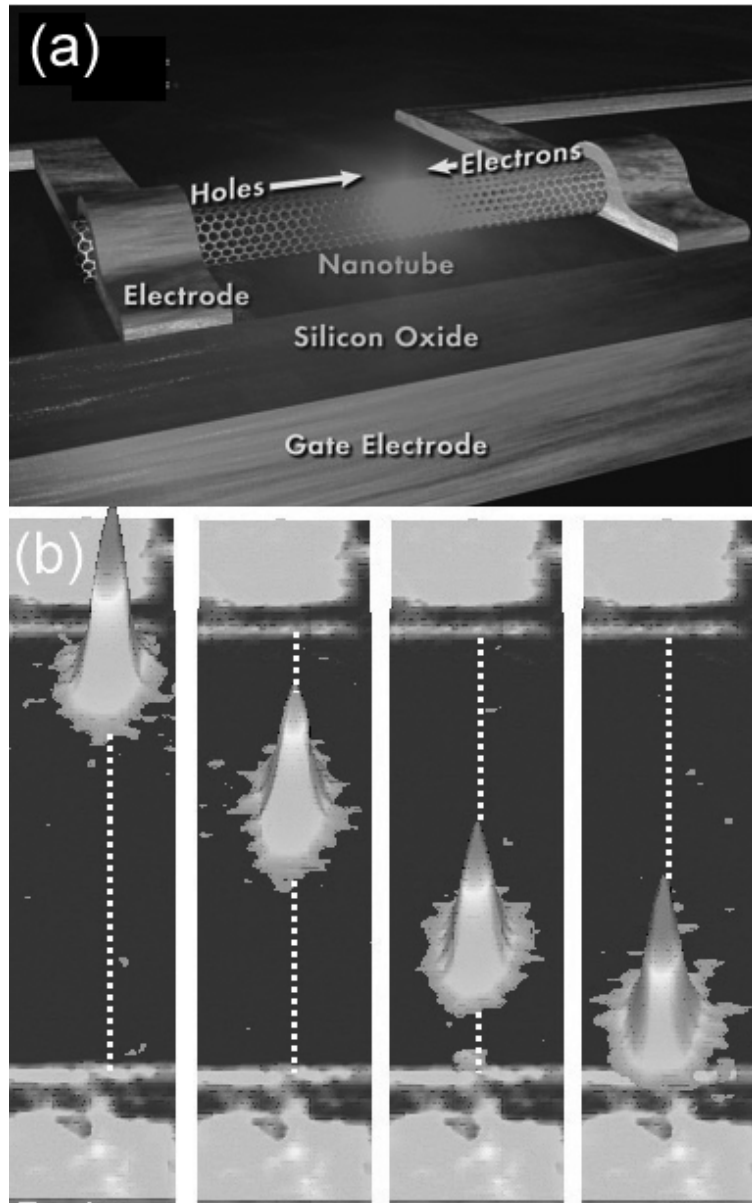


Fig. 14.17. (*Color online*) Schematic plot of a light-emitting device from a single carbon nanotube. (a) shows the device geometry and illustrates how electrons and holes are injected from the source and drain contact, respectively. The recombination via exciton intermediate states leads to the emission of infrared light. (b) For a CNFET with a long NT channel (about $50\mu\text{m}$) one can spatially resolve the regime of light emission due to electron-hole recombination [41]. The position of the spot depends on the voltage gating [41].

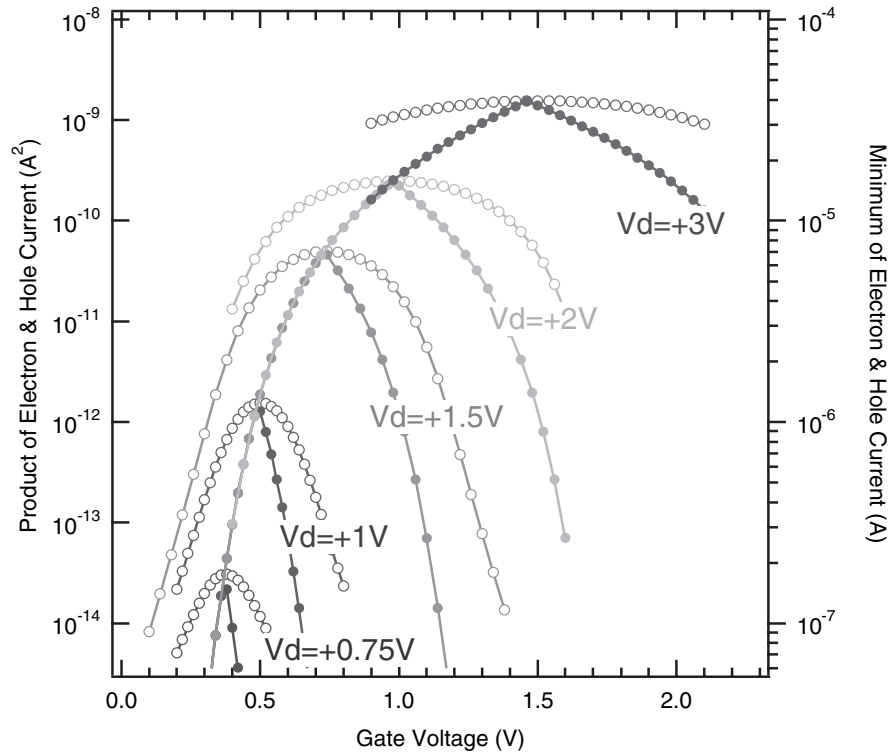


Fig. 14.18. (*Color online*) Calculated gate voltage dependence of the number of emitted photons from a CNFET with $t_{\text{ox}} = 2$ nm at different drain voltage (compare Fig. 14.15(a) and (b) for electrical characteristics). Open circles correspond to the inefficient recombination model (product of electron and hole current, left axis) while filled circles denote the efficient recombination model (minimum of electron and hole current, right axis).

spectrum of the light emitted from a CNFET [42]. Due to the confinement of electron-hole pairs on the cylindrical nanotube the Coulomb interaction is very strong resulting in excitons with large binding energies. Perebeinos et al. have used a tight-binding model to derive explicit scaling laws for the exciton binding energies with nanotube radius, effective mass, and dielectric constant of the oxide [43]. Concerning the recombination mechanism, these calculations suggest that the direct interband transition is weakened and the transition via an exciton state dominates light-emission. Thus the measured photon energy is determined by the bandgap reduced by the exciton binding energy which can be up to several 100 meV. Such large binding energies have been confirmed by very accurate but computationally intensive *ab-initio* calculations of excitons performed for selected carbon nanotubes [44, 45].

By spatially resolving the light emission from a long channel device (about $50\ \mu\text{m}$), Freitag et al. [41] have very recently demonstrated that electron-hole recombination occurs only in a small portion of the NT (see Fig. 14.17(b)). This novel approach to map the ambipolar domain of a CNFET is very promising for future studies as it gives complementary information to existing transport data. In combination with simulations a more detailed understanding of transistor action in one-dimensional devices may be possible.

14.3 Conclusions and Outlook

Carbon nanotube electronics remains a very promising route to solve future down-scaling problems of conventional silicon technology. Field-effect transistors with performance that is competitive to state-of-the-art devices [4–6] and even logic gates from single nanotubes [8] have been demonstrated. However, the physics of carbon nanotube electronic devices can be quite different from conventional ones. In particular, carbon nanotubes show ballistic transport over typical device length [6, 7], they have electronic properties linked to their structure [1], and their cylindrical quasi-one-dimensional structure leads to unusual electrostatics e.g. weak screening and no Fermi level pinning [17, 28].

For transistor action in CNFETs Schottky barriers at the metal-nanotube interface play a crucial role [9–13]. Already semiclassical transport models explain key observations of CNFETs such as the effect of gas adsorption [11]. Consequences are the importance of contact geometry for high performance, unusual scaling relations as the device size is reduced [14, 34], and leakage currents due to injection of minority charge carriers at the drain contact [38]. The device physics of CNFETs allows performance control by new parameters e.g. by the material of the metal electrodes which determines the SB height. On the other hand, limitations unknown in conventional transistors occur [34, 38] and require new device designs [39, 40]. To eliminate SBs at the metal-nanotube contacts is a key challenge for future research. For small bandgap nanotubes Javey et al. have recently achieved negligible small barriers by choosing Palladium or Aluminum electrodes [6, 21]. However, the understanding of the favorable contacts is still limited and remains an important issue for further investigations. Controlled doping of the contacts [22] or new device designs [23, 39, 40] may provide a different route to enhanced performance of CNFETs.

Due to their unique optical properties such as equal effective masses of electrons and holes and tunable bandgap carbon nanotubes can be utilized in novel nanoscale optoelectronic devices such as light emitters [15] or photo detectors [24]. We have shown that light emission can be observed from a CNFET by an appropriate choice of gate and drain voltages due to the simultaneous injection of electrons and holes [15]. From the transport models developed for CNFETs we can explain the experimental data and estimate the optimization potential by future down-scaling of the devices. Modelling

of the electron-hole interaction, on the other hand, demonstrates that light emission occurs predominantly via the formation of excitons which can have large binding energies due to the quasi-1D electrostatics [43–45]. Very recent studies have even allowed to spatially resolve the position of light emission for long channel devices [41]. Future research along those lines will provide a wealth of complementary information on transport in 1D devices.

Carbon nanotube electronics still faces a number of serious problems such as the fabrication of large scale arrays of devices before becoming a serious technological alternative to silicon devices. However, considering the short time CNFETs have been investigated the achieved results are very impressive and fuel the hope of powerful carbon nanotube based nanoelectronics. For example, the possibility to use the same carbon nanotube transistor as an electronic or optoelectronic device depending on the applied voltages opens the door to new applications.

Acknowledgements

One of us (S.H.) thanks the Deutsche Forschungsgemeinschaft and the Stifterverband für die Deutsche Wissenschaft for financial support.

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