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A NEW FPGA BASED TIMING SYSTEM AT ELSA

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Abstract

At the electron stretcher facility ELSA a beam intensity upgrade from 20 mA to 200 mA is in progress. Investigations showed, that the maximum beam current is currently limited by excitation of beam instabilities. For separated characterization of single bunch instabilities from multi-bunch ones, a high beam current stored in a single revolving bunch is required. These high beam currents can only be achieved by accumulation of many shots from the injector.

The existing timing system is not capable of single bunch injection and accumulation in the main stretcher ring. Therefore a new FPGA based timing system, synchronized to the RF system of the accelerator, has been developed which will completely supersede the existing one. Simultaneously the "slow" timing system, providing trigger signals for the typically 6 s long accelerator cycle, is also modernized using a similar FPGA based solution to achieve a much better duty cycle during standard operation.

In this contribution the FPGA designs laying the focus on the single bunch accumulation will be presented.

ELSA

The electron stretcher facility ELSA (see Fig. 1) is a three stage accelerator consisting of two linear accelerators and a fast ramping booster synchrotron which are utilized as injector for the main storage ring. In the storage ring electrons can be accumulated by multiple injections of the booster, post-accelerated to a maximum energy of 3.2 GeV and then be extracted to one of the hadron physics experiments *Crystal Barrel* or *BGO-OD*. The typical cycle length is 6 s consisting of 400 ms injection time and 2×300 ms acceleration/deceleration time. The extraction takes place during the remaining 5 s, where the electrons are extracted using a third integer resonance, resulting in a constant electron current of typically up to 2 nA at the experiments.

Motivation

The ELSA stretcher ring is currently operated with a maximum current of 20 mA. That allows for an extraction of currents of about 2 nA during an extraction time of typically 5 s. The experiments desire an increase of this current by a factor of 10. In order to preserve the duty factor of > 80 % the intensity of the beam accumulated in the storage ring has to be increased by one order of magnitude to 200 mA.

The maximum beam current that can be stored is limited by emerging beam instabilities. These can be classified in single- and multi bunch instabilities. The latter ones are damped by the installed three dimensional bunch-by-bunch feedback system [1] whereas the investigation of single bunch instabilities requires the accumulation of a single bunch in the accelerator.

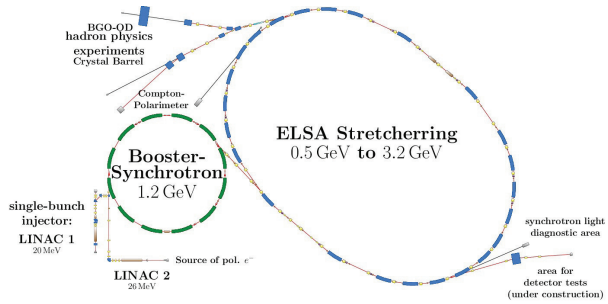

Figure 1: Sketch of the electron stretcher facility ELSA.

At the moment this can only be achieved by excitation and subsequently removing all unwanted bunches of a homogeneously filled accelerator ring. Unfortunately the attainable current per single bunch is then limited to approximately 800 µA/bunch by multi bunch instabilities occurring during injection.

To workaround these limitations a new high current single bunch injector, LINAC1 [2], is currently under construction. In the *short pulse mode* only a single bucket in the booster synchrotron can be filled whereas in *long pulse mode* it is capable of filling the whole synchrotron with a high intensity beam.

Besides the ability to accumulate electrons into a single bunch in the stretcher ring it will also be possible to produce any arbitrary filling pattern in the stretcher ring by successive injection into different buckets. This is in particular very helpful for investigations of instabilities caused by trapped ions [3].

CURRENT TIMING SYSTEM

The timing system can be separated into two different branches. The so-called *fast timing* system is operated at 50 Hz line frequency generating trigger signals for timing the injector (gun and linear accelerator) and accumulation in the stretcher ring. Due to the fluctuating line frequency the acceleration cycle in the booster synchrotron is not static. The trigger for the injector (gun and LINAC) is generated by a premagnetized peaking strip[1] placed in the magnet gap of the booster's dipole.

With the current setup there is no synchronization to the revolution clock, therefore the filled bucket in the booster synchrotron is unknown. In addition the transfer to the stretcher ring is not synchronized as well, making it impossible to accumulate electrons in a single bucket or even produce a requested filling pattern.

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[1] ferromagnetic material with an almost rectangular hysteresis loop

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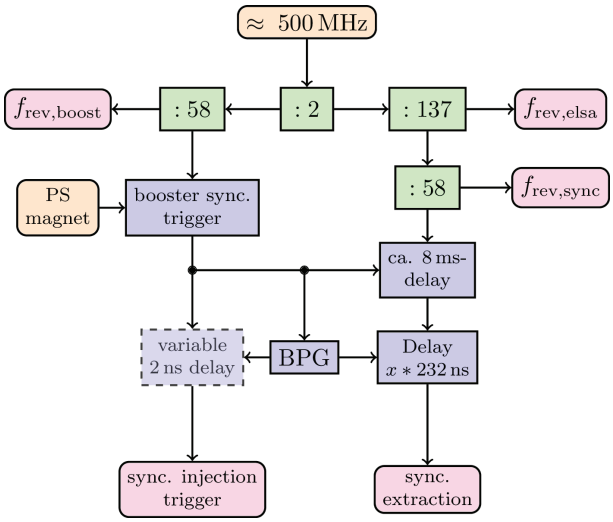

Figure 2: FPGA design of the new *fast timing* system.

The *slow timing* is used for defining the overall acceleration cycle and delivering trigger pulses to the hardware (e.g. for ramping the magnet power supplies to their extraction energy). It is currently set up with two remotely programmed digital pulse delay units *DG535* by *Stanford Research Systems*. A major drawback is the resulting static trigger sequence only allowing a fixed number of accumulation shots into the stretcher ring, regardless of the actually needed number of shots to reach the desired current.

FAST TIMING

For single bunch accumulation a complete renewal of the timing system is required. A new Xilinx Spartan 6 FPGA based solution is being set up. An overview of the FPGA design is shown in Fig. 2.

For bucket synchronization its clock is directly locked to half the master RF frequency of $f_{HF} \approx 500\,\text{MHz}$. The required revolution clock for the booster ($f_{rev,boost} \approx 4.3\,\text{MHz}$) is synthesized by a PLL[2] taking into account the harmonic number of $h_{boost} = 116$. For the stretcher ring ($f_{rev,ELSA} \approx 1.8\,\text{MHz}$, $h_{ELSA} = 274$) it is derived by a counter frequency divider implemented in logic due to limitations of the PLL. The generated clock signals are also routed outside the FPGA to allow other components to synchronize on these revolution clocks.

In single bunch operation mode, the peaking strip signal firing the electron pulse generation, is aligned to the booster revolution clock in order to always fill the same bucket. This trigger can be optionally delayed by 2 ns[3] to fill an even bucket instead of an odd one[4].

The extraction trigger from the booster is derived by delaying the injection trigger by ≈ 8 ms. Furthermore it is synchronized to a coinciding clock of both revolution clocks to allow extraction always into the same bucket. Due to the different harmonic numbers this coincidence rate is only ≈ 31.5 kHz.

Arbitrary filling patterns can be generated by delaying the extraction again by a multiple of the revolution time in the booster. The number of revolutions needed is pre-calculated and stored together with the number of shots into a lookup table called *bunch pattern generator* (BPG). The BPG also controls the variable 2 ns delay in the injection path to allow for accumulation into even and odd buckets.[5] The injection efficiency is not affected by the additional delays of in total[6] 63 µs due to the huge energy acceptance of the stretcher ring.

All outputs are supplied with configurable delays with a step size of 4 ns with a span from 4 ns to 1 ms for fine adjustment of the trigger pulses.

The delays, operational mode and the bunch patterns can be directly configured from the control system by writing to 32 bit control registers using a serial communication interface. An online programmable memory block allows for storage of arbitrary bunch patterns with a resolution of 23 bits of shots per bucket.

To reduce development cost of the overall system, it was decided to use a commercially available FPGA development board (see Fig. 3). It can be extended by a so called *mezzanine card* as an expansion. In order to support the signaling standard of the existing hardware such a mezzanine board has to be developed for level shifting from *LVDS* to *TTL*.

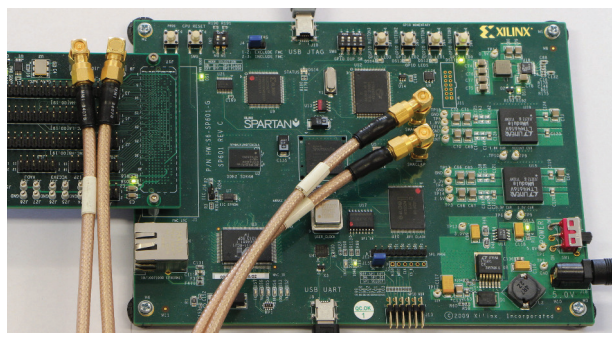

Figure 3: Xilinx Spartan 6 development board used for the timing system. The mezzanine card on the left will be replaced by an in-house developed board for level shifting from LVDS to TTL.

SLOW TIMING

The slow timing module will be set up using the same FPGA board as being used for the fast one. But in contrast it is only used as a trigger sequence generator. Its purpose is to replace the static timing provided by the two digital pulse delay units. Therefore the static sequence will be split up into three parts (see Fig. 4): In the first part the *fast timing* system takes care of the injection and signals the

[2] Phase Locked Loop circuit integrated into the FPGA's Clock Management Tile (CMT).
[3] The bucket distance
[4] The name *even* or *odd* bucket is rather arbitrary here.
[5] Without, only odd buckets could be filled due to the even harmonic numbers in both accelerators.
[6] Worst case scenario: 31.8 µs delay due to synchronization plus 31.5 µs delay in favour of the filling pattern.

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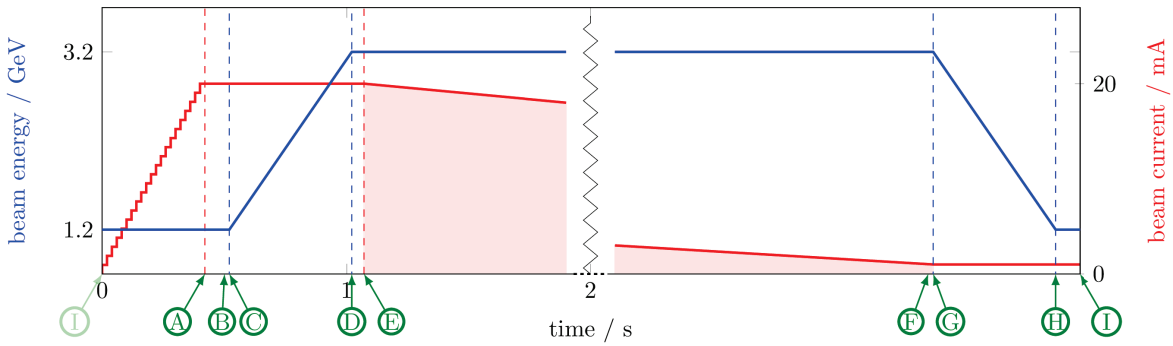

Figure 4: Cycle of the main stretcher ring.

slow timing the completion of injection. Afterwards triggers for the hardware to initiate the energy ramp and following extraction are generated.

The last part, stopping extraction and ramping down to injection energy, can either be executed after a fixed amount of time (reproducing the current setup) or be executed right after the stored current in the stretcher ring falls under a given threshold. This is useful to automatically adapt to new extraction durations depending on the extracted current desired by the experiments and thus always to maximize the duty cycle.

With an integrated switch matrix (see Tab. 1) the generated triggers can be routed to the hardware. Also eight additional signals can be fired at an arbitrary position in the cycle for additional diagnostic hardware triggering, i.e. triggering a streak camera together with beam excitation by a stripline kicker during the energy ramp.

Table 1: Planned trigger signals vs. target device (routing matrix); • default operation mode, ○ freely selectable trigger source. Compare triggers to Fig. 4.

trigger \ output to	Main Magnets	Corrector Magnets	RF Ramp	8× Arb. diag. trig.	Exp. spill start	Exp. spill stop	Fast Timing System
ramp prep. (B)	•			○			
ramp up (C)	•	•	•	○			
ramp done (D)				○			
extr. start (E)				○	•		
ramp prep. (F)	•			○			
ramp down (G)	•	•	•	○		•	
ramp done (H)				○			
injection prep. (I)				○			
enable injection				○			•

OUTLOOK

The basic FPGA design of the *fast timing* system is completed. It is currently tested with reduced harmonic numbers of 8 and 10 and a simulated input trigger signal for the peaking strip. As clock source the internal 200 MHz oscillator of the development board is used. Also the bunch pattern generator is implemented and is working as expected. The next step is the layout of the mezzanine card for signal conversion of the trigger outputs and clock reconstruction from the RF master frequency as supply for the FPGA.

The concept for the *slow timing* is completed and currently under design. It will significantly improve the machine operation especially in storage mode by replacing the old software controlled design.

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